MODULE SPECIFICATION

Model:ZEN-BDM90

Yancan Electronic Technology

1. Overview

1.1 Features

- ✧ Bluetooth specification V4.2 compliant
- ✧ BR 1Mbps, EDR 3Mbps, LE 1Mbps data rate
- ✧ LE profiles supported: GATT, HID over GATT (HOGP), Beacon
- ✧ Classic Bluetooth profiles supported: SPP, A2DP, HFP 1.6 with WBS, HID, PBAP, AVRCP, HSP, OBEX
- ✧ UART or OTA firmware upgrade
- ✧ Serial port command for applications

1.2 Applications

- ✧ Bluetooth SPP or BLE to TTL serial data conversion
- ✧ Bluetooth wireless data transmission
- ✧ Medical and industrial telemetry
- ✧ Portable printers
- ✧ Barcode scanning devices
- ✧ Mobile POS devices
- ✧ Smart appliances
- ✧ Industrial automation
- ✧ Custom Bluetooth audio devices

1.3 Descriptions

The Module ZEN-BDM90 has a notable merit that its firmware supports concurrent Bluetooth SPP and GATT connections. It establishes a Bluetooth bidirectional communication channel which is between the application MCU and the mobile phone through the UART interface. The application MCU can send a corresponding command to enable the Bluetooth module and to set it into different modes, then to send and receive communication data at the SPP or GATT level. The MCU can also read the mode status of the module through serial commands.

This module is designed with Cypress® CYW20706 dual mode Bluetooth 5.0 SoC. CYW20706 features

96 MHz Cortex M3 core, excellent receiving sensitivity down to -96 dBm (BLE GFSK), integrated PA to support Class 1 Tx power up to 12 dBm. These two RF parameters contribute to its best in class link budget to enable long Bluetooth communication distance around 100 meters or even farther. This module has a fine tuned inverted-F PCB antenna. It provides excellent efficiency while keeps small size. This module can be easily integrated in a product board.

As a dual mode Bluetooth module, it can realize both GATT and SPP connections concurrently, which provide the best interoperability for various iOS and Android mobile devices. It supports both BR (2 Mbps) and EDR (3 Mbps) when running SPP. These high Classic Bluetooth data

rate provides high throughput, enabling applications which require higher throughput than what BLE can provide. Its raw data throughput running SPP can reach up to 1 Mbps.

This module also supports Bluetooth audio profiles including but not limited to A2DP, HFP, and AVRCP. An external audio codec can be flexibly connected via PCM interface to drive a speaker and a microphone. This module can also support iAP2 and HomeKit for MFi licensed developers.

The module comes with a set of AT commands via UART interface for setting up a bidirectional Bluetooth data link easily between an application MCU and mobile phones.

1.4 Functional Block Diagram

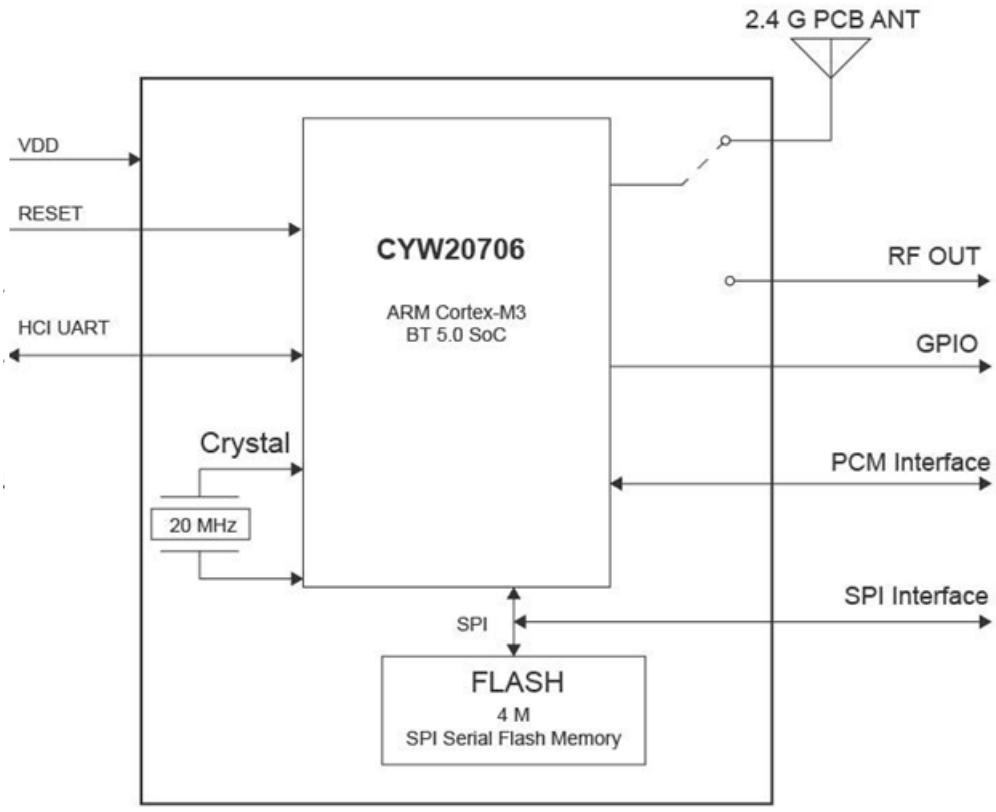

Figure 1. Functional Block Diagram

2. Pin Configuration and Functions

2.1 Module Pin Diagram

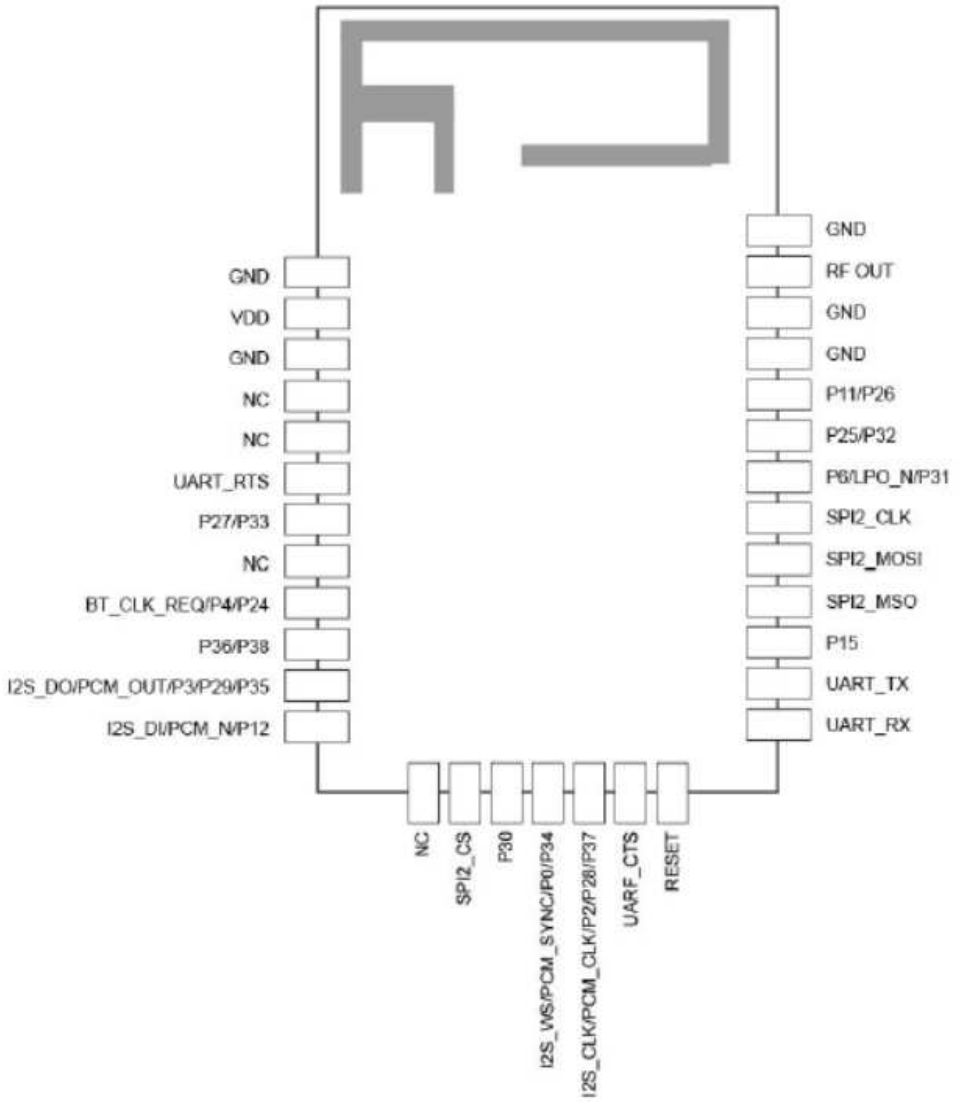

Figure 2 Pin diagram

2.2 Pin Functions

Pin	Name	I/O	Description
1	GND	power	Power supply: ground
2	VDD	power	Power supply: DC+2.7V~3.6V
3	GND	power	Power supply: ground
4	NC	--	No connection
5	NC	--	No connection
6	UART_RTS	IO	UART request to send output
7	P27(PWM1)	input	GPIO: P27 SPI_1: MOSI (master and slave) Optical control output: QOC1

Pin	Name	I/O	Description
			Triac control 2 *Current: 16 mA sink*
	P33	input	GPIO: P33 A/D converter input 6 Quadrature: QDX1 SPI_1: MOSI (slave only) Auxiliary clock output: ACLK1 Peripheral UART: puart_rx
8	NC	--	No connection
9	BT_CLK_REQ	output	This pin is used for shared-clock applications.
	P4	input	GPIO: P4 Quadrature: QDY0 Peripheral UART: puart_rx SPI_1: MOSI (master and slave) IR_TX
	P24	input	GPIO: P24 SPI_1: SPI_CLK (master and slave) Peripheral UART: puart_tx
10	P36	input	GPIO: P36 A/D converter input 3 Quadrature: QDZ0 SPI_1: SPI_CLK (master and slave) Auxiliary Clock Output: ACLK0 External T/R switch control: ~tx_pd
	P38	input	GPIO: P38 A/D converter input 1 SPI_1: MOSI (master and slave) IR_TX
11	I2S_DO/PCM_OUT	IO	PCM/I2S data output
	P3	input	GPIO: P3 Quadrature: QDX1 Peripheral UART: puart_cts SPI_1: SPI_CLK (master and slave)
	P29(PWM3)	input	GPIO: P29 Optical control output: QOC3 A/D converter input 10 LED2 *Current: 16 mA sink*
	P35	input	GPIO: P35 A/D converter input 4 Quadrature: QDY1 Peripheral UART: puart_cts BSC: SDA
12	I2S_DI/PCM_IN	IO	PCM/I2S data input
	P12	input	GPIO: P12 A/D converter input 23

Pin	Name	I/O	Description
13	NC	--	No connection
14	SPI2_CS	IO	Serial flash active-low chip select
15	P30	Input	GPIO: P30 A/D converter input 9 Peripheral UART: puart_rts
16	I2S_WS/PCM_SYNC	IO	PCM sync/I2S word select
	P0	input	GPIO: P0 A/D converter input 29 Peripheral UART: puart_tx SPI_1: MOSI (master and slave) IR_RX 60Hz_main *Note: Not available during TM1 = 1.*
	P34	input	GPIO: P34 A/D converter input 5 Quadrature: QDY0 Peripheral UART: puart_rx External T/R switch control: tx_pd
17	I2S_CLK/PCM_CLK	IO	PCM/I2S clock
	P2	input	GPIO: P2 Quadrature: QDX0 Peripheral UART: puart_rx SPI_1: SPI_CS (slave only) SPI_1: MOSI (master only)
	P28(PWM2)	input	GPIO: P28 Optical control output: QOC2 A/D converter input 11 LED1 *Current: 16 mA sink*
	P37	input	GPIO: P37 A/D converter input 2 Quadrature: QDZ1 SPI_1: MISO (slave only) Auxiliary clock output: ACLK1 BSC: SCL
18	UART_CTS	IO	UART clear to send input
19	RESET	input	Reset input, active low
20	UART_RX	IO	UART receive data
21	UART_TX	IO	UART transmit data
22	P15	input	GPIO: P15 A/D converter input 20 IR_RX

Pin	Name	I/O	Description
			60Hz_main
23	SPI2_MISO	IO	BSC clock
24	SPI2_MOSI	IO	BSC data
25	SPI2_CLK	IO	Serial flash SPI clock
26	P6(PWM2)	input	GPIO: P6 Quadrature: QDZ0 Peripheral UART: puart_rts SPI_1: SPI_CS (slave only) 60Hz_main
	LPO_IN	input	External LPO input
	P31	input	GPIO: P31 A/D converter input 8 Peripheral UART: puart_tx
27	P25	input	GPIO: P25 SPI_1: MISO (master and slave) Peripheral UART: puart_rx
	P32	input	GPIO: P32 A/D converter input 7 Quadrature: QDX0 SPI_1: SPI_CS (slave only) Auxiliary clock output: ACLK0 Peripheral UART: puart_tx
28	P11	input	GPIO: P11 Keyboard scan output (column): KSO3 A/D converter input 24
	P26(PWM0)	input	GPIO: P26 SPI_1: SPI_CS (slave only) Optical control output: QOC0 Triac control 1 *Current: 16 mA sink*
29	GND	power	Ground
30	GND	power	Ground
31	RFOUT	output	RF antenna port
32	GND	power	Ground

3. Specifications

3.1 Absolute Maximum Ratings

Caution! The absolute maximum ratings in the following table indicates voltages levels where permanent physical damage to the device can occur, even if these limits were exceeded for only a brief duration.

Param.	Specification			Unit
	Min.	Typ.	Max.	
VDD	-0.5	3	3.795	V
Ambient Temperature	-30	--	+85	℃
Storage Temperature	-40		+125	℃

3.2 RF Characteristics

3.2.1 Transmitter RF Parameters

Param.	conditions	Min.	Typ.	Max.	Unit
General					
Frequency Range	-	2402	-	2480	MHz
Class1: GFSK TX Power	-	-	12	-	dBm
Class1: EDR TX Power	-	-	9	-	
Class2: GFSK TX Power	-	-	2	-	
Power Control Step	-	2	4	8	
Modulation Accuracy					
π/4-DQPSK Frequency Stability	-	-10	-	10	kHz
π/4-DQPSK RMS DEVM	-	-	-	20	%
π/4-QPSK Peak DEVM	-	-	-	35	%
π/4-DQPSK 99% DEVM	-	-	-	30	%
8-DPSK Frequency Stability	-	-10	-	10	kHz
8-DPSK RMS DEVM	-	-	-	13	%
8-DPSK Peak DEVM	-	-	-	25	%
8-DPSK 99% DEVM	-	-	-	20	%
In-Band Spurious Emissions					
1.0 MHz < |M-N| < 1.5 MHz	-	-	-	-26	dBm
1.5 MHz < |M-N| < 2.5 MHz	-	-	-	-20	dBm
|M-N| ≥ 2.5 MHz	-	-	-	-40	dBm
Out-of-Band Spurious Emissions					
30 MHz ~ 1 GHz	-	-	-	-36	dBm
1 GHz ~ 12.75 GHz	-	-	-	-30	dBm
1.8 GHz ~ 1.9 GHz	-	-	-	-47	dBm
5.15 GHz ~ 5.3 GHz	-	-	-	-47	dBm

Param.	conditions	Min.	Typ.	Max.	Unit
GPS Band Noise Emissions (Without a front-end band filter)					
1572.92 MHz ~ 1577.92 MHz	-	-	-150	-127	dBm/Hz
Out-of-Band Noise Emissions (Without a front-end band filter)					
65 MHz ~ 108 MHz	FM RX	-	-145	-	dBm/Hz
746 MHz ~ 764 MHz	CDMA	-	-145	-	dBm/Hz
869 MHz ~ 960 MHz	CDMA	-	-145	-	dBm/Hz
925 MHz ~ 960 MHz	EDGE/GSM	-	-145	-	dBm/Hz
1805 MHz ~ 1880 MHz	EDGE/GSM	-	-145	-	dBm/Hz
1930 MHz ~ 1990 MHz	PCS	-	-145	-	dBm/Hz
2110 MHz ~ 2170 MHz	WCDMA	-	-140	-	dBm/Hz

Note:

All specifications are for industrial temperature.

All specifications are single-ended. Unused input are left open.

+12 dBm output for GFSK measured with PA VDD = 2.5 V.

+9 dBm output for EDR measured with PA VDD = 2.5 V. Maximum value is the value required for Bluetooth qualification. Meets this spec using a front-end bandpass filter

3.2.2 Receiver RF Parameters

Param.	conditions	Min.	Typ.	Max.	Unit
General					
Frequency Range	-	2402	-	2480	MHz
RX Sensitivity	GFSK, 0.1% BER, 1 Mbps	-	-93.5	-	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	-	-95.5	-	dBm
	8-DPSK, 0.01% BER, 3 Mbps	-	-89.5	-	dBm
Maximum Input	GFSK, 1Mbps	-	-	-20	dBm
Maximum Input	π/4-DQPSK, 8-DPSK, 2/3 Mbps	-	-	-20	dBm
Interference Performance					
GFSK Modulation					
C/I cochannel	GFSK, 0.1% BER	-	9.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	-	-5	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	-	-40	-30	dB
C/I ≥ 3 MHz adjacent channel	GFSK, 0.1% BER	-	-49	-40	dB
C/I image channel	GFSK, 0.1% BER	-	-27	-9	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	-	-37	-20	dB
QPSK Modulation					
C/I cochannel	π/4-DQPSK, 0.01% BER	-	11	13	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.01% BER	-	-8	0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.01% BER	-	-40	-30	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	-	-50	-40	dB
C/I image channel	π/4-DQPSK, 0.01% BER	-	-27	-7	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.01% BER	-	-40	-20	dB
8PSK Modulation					
C/I cochannel	π/4-DQPSK, 0.01% BER	-	17	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	-	-5	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	-	-40	-25	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	-	-47	-33	dB
C/I image channel	8-DPSK, 0.1% BER	-	-20	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	-	-35	-13	dB
Out-of-Band Blocking Performance (CW)					
30 MHz ~ 2000MHz	0.1% BER	-	-10	-	dBm
2000MHz ~ 2399MHz	0.1% BER	-	-27	-	dBm
2498MHz ~ 3000MHz	0.1% BER	-	-27	-	dBm
3000MHz ~ 12.75 GHz	0.1% BER	-	-10	-	dBm

Param.	conditions	Min.	Typ.	Max.	Unit
Out-of-Band Blocking Performance, Modulated Interferer					
776 MHz ~ 764 MHz	CDMA	-	-10	-	dBm
824 MHz ~ 849 MHz	CDMA	-	-10	-	dBm
1850 MHz ~ 1910 MHz	CDMA	-	-23	-	dBm
824 MHz ~ 849 MHz	EDGE/GSM	-	-10	-	dBm
880 MHz ~ 915 MHz	EDGE/GSM	-	-10	-	dBm
1710 MHz ~ 1785 MHz	EDGE/GSM	-	-23	-	dBm
1850 MHz ~ 1910 MHz	EDGE/GSM	-	-23	-	dBm
1850 MHz ~ 1910 MHz	WCDMA	-	-23	-	dBm
1920 MHz ~ 1980 MHz	WCDMA	-	-23	-	dBm
Intermodulation Performance					
BT, Df = 4MHz					
Spurious Emissions					
30 MHz ~ 1 GHz	-	-	-	-62	dBm
1 GHz ~ 12.75 GHz	-	-	-	-47	dBm
65 MHz ~ 108 MHz	FM RX	-	-147	-	dBm
746 MHz ~ 764 MHz	CDMA	-	-147	-	dBm/Hz
851 MHz ~ 894 MHz	CDMA	-	-147	-	dBm/Hz
925 MHz ~ 960 MHz	EDGE/GSM	-	-147	-	dBm/Hz
1805 MHz ~ 1880 MHz	EDGE/GSM	-	-147	-	dBm/Hz
1930 MHz ~ 1990 MHz	PCS	-	-147	-	dBm/Hz
2110 MHz ~ 2170 MHz	WCDMA	-	-147	-	dBm/Hz

Note:

All specifications are single ended. Unused inputs are left open. All specifications, except typical, are for industrial temperature.
Typical operating conditions are 3.3 V VBAT and 25 ℃ ambient temperature.
The receiver sensitivity is measured at BER of 0.1% on the device interface.

Typical GFSK CI numbers at -7 MHz, -5 MHz and -3 MHz are -45 dB, -42 dB and -41 dB, respectively.
Typical QPSK CI numbers at -7 MHz, -5 MHz and -3 MHz are -46 dB, -43 dB and -42 dB, respectively.
Typical 8PSK CI numbers at -7 MHz, -5 MHz and -3 MHz are -50 dB, -45 dB and -45 dB, respectively. Meets this specification using front-end band pass filter.
Numbers are referred to the pin output with an external BPF filter.

F0=-64 dBm Bluetooth-modulated signal, f1=-39 dBm sine wave, f2=-39 dBm Bluetooth-modulated signal, f0=2f1-f2, and |f2-f1|=n*1 MHz, where n is 3, 4 or 5. For the typical case, n=4.
Includes baseband radiated emissions.

3.2.3 Antenna Requirements

The module has alternative internal PCB antenna (antenna gain: -2.3 dBi) and external antenna.

3.3 Power Consumption

Current consumption (under ambient temperature, the power supply is 3.0 V).

Conditions	Current(mA)
Receive (1 Mbps) current level when receiving a basic rate packed (TBD mA).	12.5
Transmit (1 Mbps) current level when transmitting a basic rate packet.	26.5
Receive (EDR) current level when receiving 2 or 3 Mbps rate packet.	12.5
Transmit (EDR) current level when receiving 2 or 3 Mbps rate packet.	20.0
DM1/DH1 average current during a basic rate maximum throughput connection that includes only this packet type.	14.5
DM3/DH3 average current during a basic rate maximum throughput connection that includes only this packet type.	17.0
DM5/DH5 average current during a basic rate maximum throughput connection that includes only this packet type.	17.5
HV1 average current during an SCO voice connection consisting of only this packet type. The ACL channel is in 500ms Sniff.	14.0
HV2 average current during an SCO voice connection consisting of only this packet type. The ACL channel is in 500ms Sniff.	9.0
HV3 average current during an SCO voice connection consisting of only this packet type. The ACL channel is in 500ms Sniff.	7.0
Sleep UART transport active. External LPO clock available.	0.120
Inquiry Scan (1.28 sec.). periodic scan rate is 1.28 sec.	0.188
Page Scan (R1) Periodic scan rate is R1 (1.28 sec.).	0.188
Inquiry Scan + Page Scan (R1), both inquiry and page scan are interlaced at a 1.28 seconds periodic scan rate.	0.286
Sniff master (500 ms) attempt and timeout parameters set to 4. Quality connection that rarely requires more than a minimum packet exchange.	0.415
Sniff slave (500 ms) attempt and timeout parameters set to 4. Quality connection that rarely requires more than a minimum packet exchange.	0.408
Sniff (500 ms) + Inquiry or Page Scan (R1)	0.700
Sniff (500 ms) + Inquiry Scan + Page Scan (R1)	0.800

Note:

The values in this table were calculated for a 90% efficient DC-DC at 3V in HCI mode, and based on a Class 1 configuration bench-marked at Class2. Lower values are expected for a Class2 configuration using an external LPO and corresponding PA configuration.

4. Application and Layout

4.1 Application Block Diagram

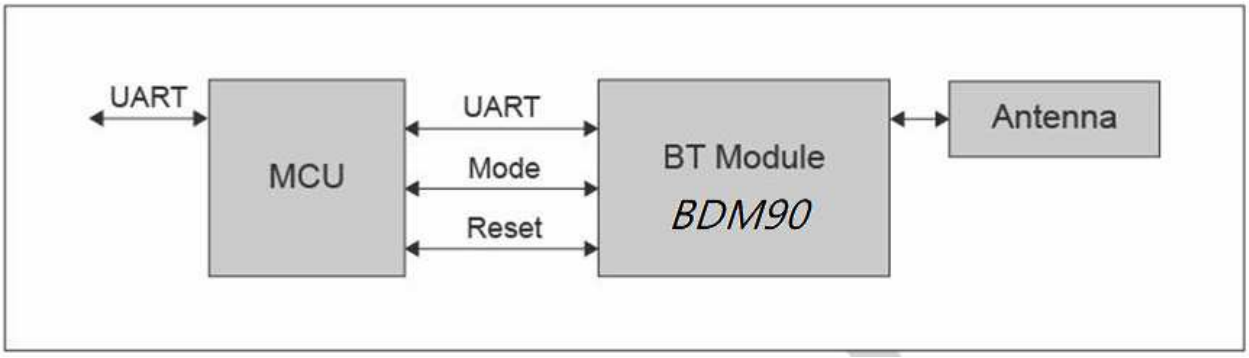

Figure 3. Application Block Diagram

4.2 Typical Application Schematic

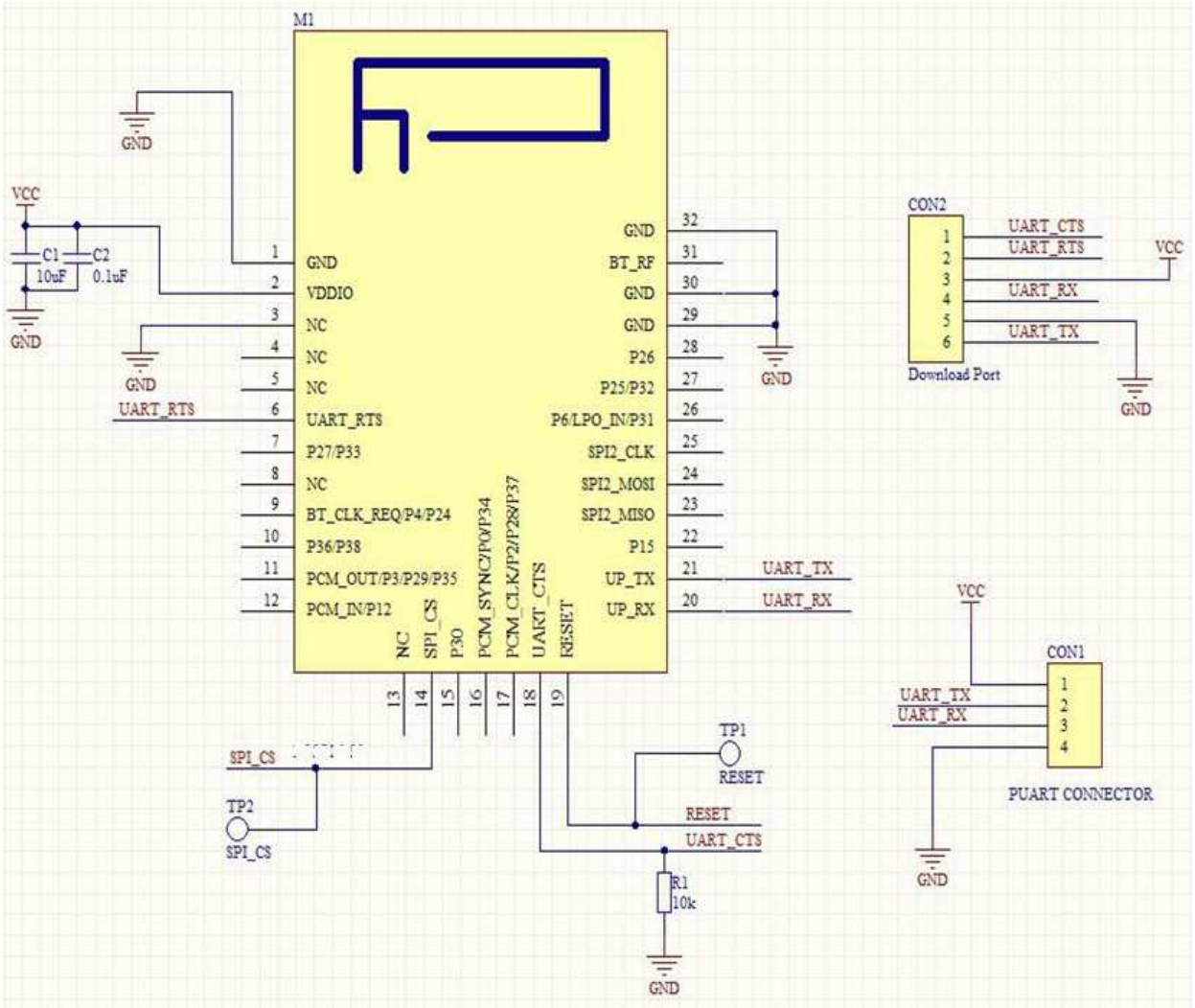

Figure 4. Typical Application Schematic

Note: When using PUART, UART_CTS signal must be pulled down to the ground.

4.3 Layout Guideline

1. The antenna needs to have enough clearance area.
2. The filter capacitor should be as close as possible to the module.
3. Do not place strong interference lines under the module.

5. Mechanical and Package

5.1 Module Size

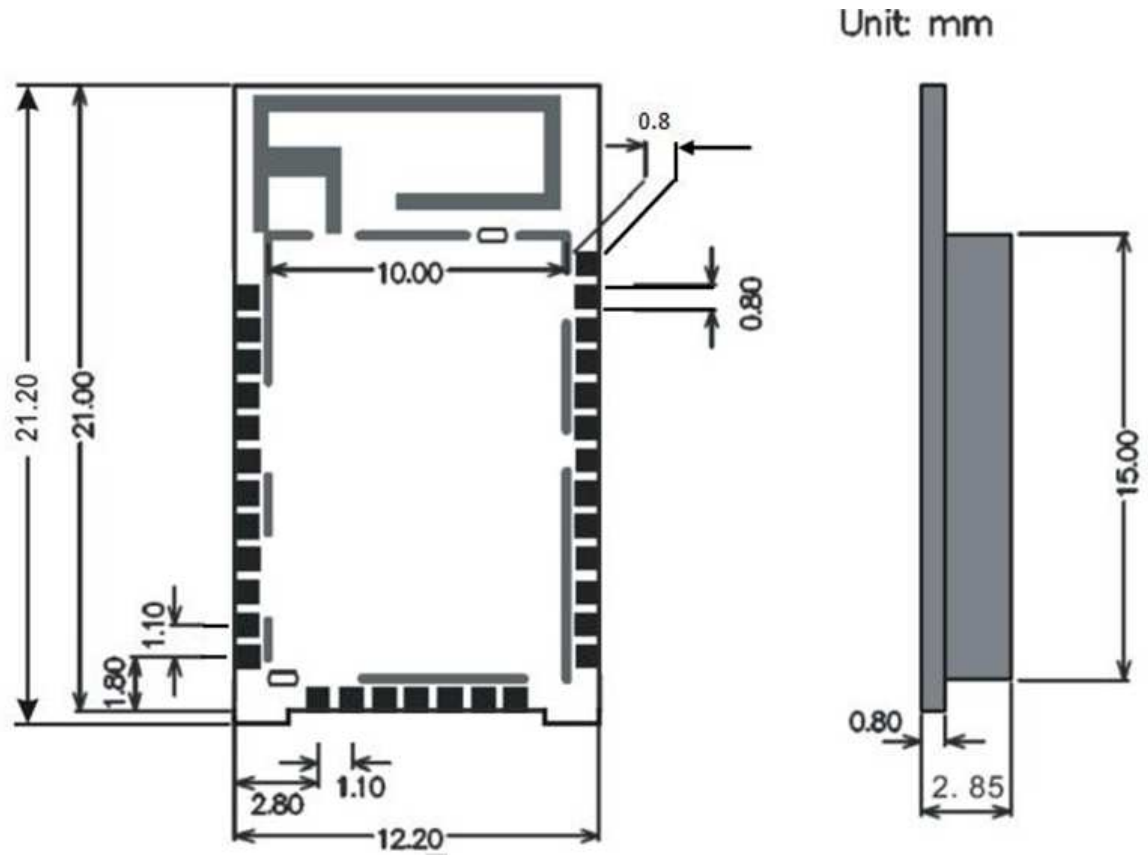

Figure 5. Module Size

5.2 Recommended PCB Footprint

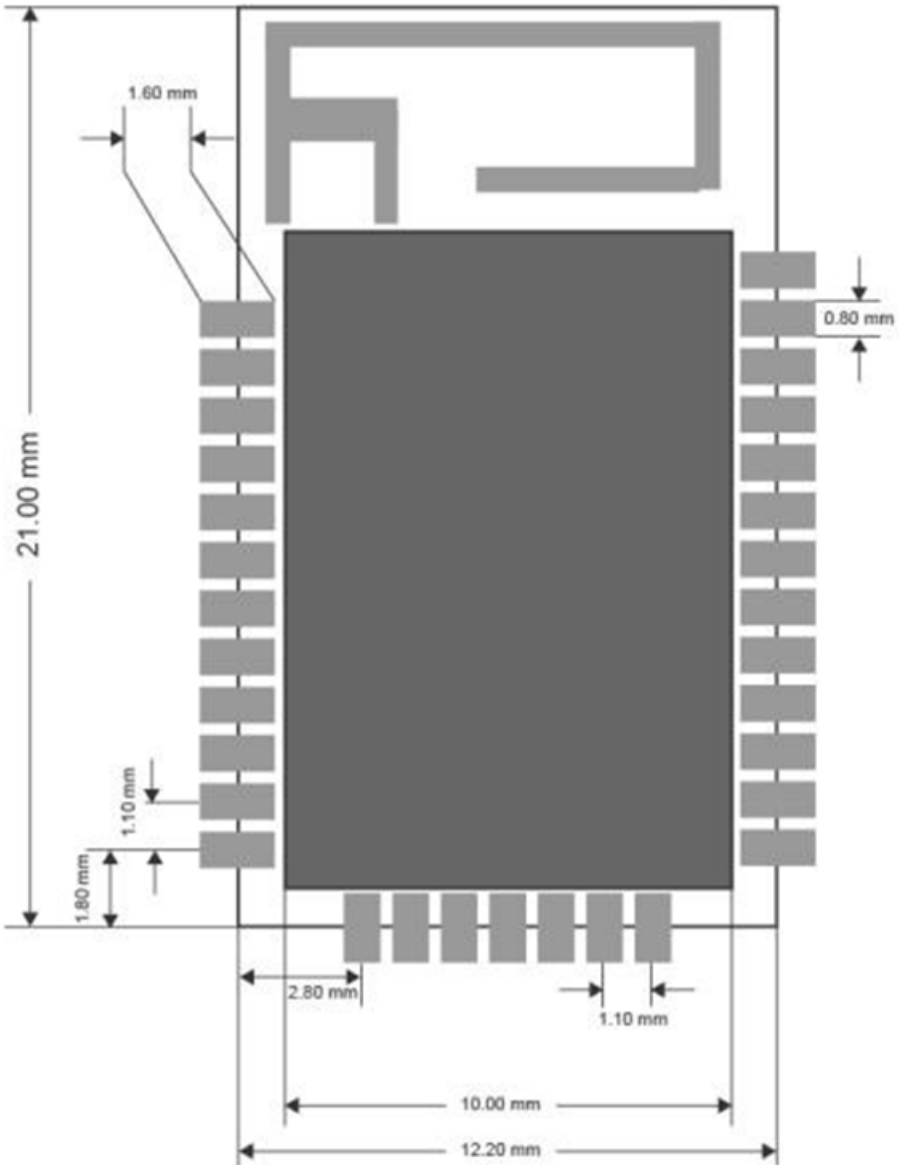

Figure 6. Recommended PCB Footprint

Note:

1. The area of the product board under the module antenna needs to be clear of metal ground or traces.
2. The decoupling capacitor for 3P3VD input should be as close to the module as possible.
3. Strong interference line at the bottom of the module should be forbidden.

6. Thermal Reflow

Referred to IPC/JEDEC standard.
Peak temperature: < 250°C
Number of times: ≤ 2

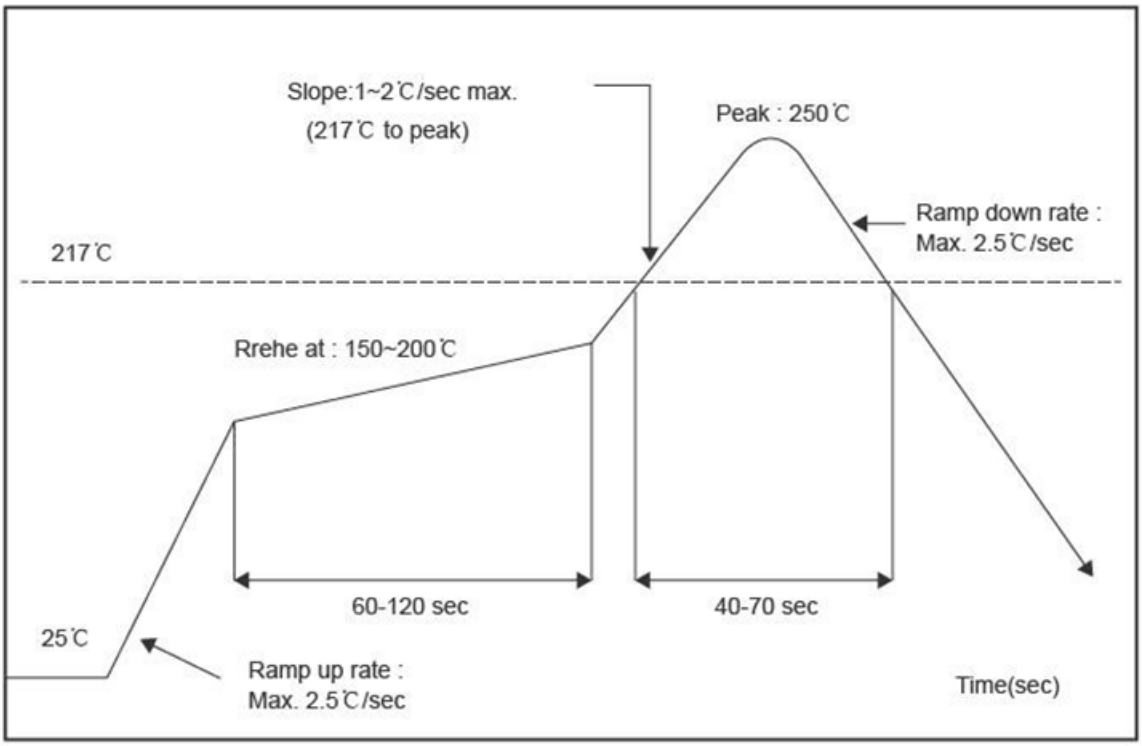

Figure 7. Recommended Reflow for Lead Free Solder

Note: The module is recommended not to go through reflow oven twice

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